National PhD in Micro- and Nano-Electronics

SEMINAR

Electronics for Massively Parallel Brain-Computer Interfaces

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Abstract: Brain-computer interfaces (BCIs) of the future will be used to treat neurological disorders for which a cure does not exist yet. For this futuristic view to become a reality, we must overcome many technological challenges. A major goal is to increase the number of neurons that we can simultaneously interact with. To do so, future systems will record from tens of thousands of channels at the same time. These systems will create a massive amount of raw data that needs to be compressed on the implant to lower the power consumption of the wireless data link. As custom signal specifications for BCI applications become clearer and are diverging from those needed for basic neuroscience, there is an opportunity for application-specific accelerators that improve further the power efficiency of these implants. In this talk, I will present two recent chips that perform on-chip lossy compression and spike sorting. Together, these solutions provide analog-to-information conversion for 1024 channels with <1 µW/channel. I will also describe how this recording strategy can scale to even higher channel count, enabling the next generation of massively parallel BCIs.

Bio: Dante G. received a B.Sc. and an M.Sc. degree in Electrical Engineering from Politecnico of Turin, Italy in 2012 and 2013, respectively. He received a Ph.D. degree in Microelectronics from the University of Pavia, Italy in 2017 in the Integrated Microsystems Lab. From 2015 to 2016, he was a Visiting Scholar at Microsystems Technology labs at the Massachusetts Institute of Technology, USA. From 2016 to 2020, he was a Postdoctoral Fellow at Stanford University, USA. He is the recipient of the Wu Tsai Neurosciences Institute Interdisciplinary Scholar Award. Since 2020, he is an assistant professor in the Bioelectronics Section at Delft University of Technology, Netherlands, where he leads the Smart Brain Interfaces group. His group investigates hardware and system solutions for high-bandwidth brain-machine interfaces that can interact with the nervous system at natural resolution. They contribute solutions for massively parallel bidirectional interfaces, on-chip neural signal processing, and wireless power and data transfer.

Organizer	**Ph.D. Coordinator**
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Seminar in English
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