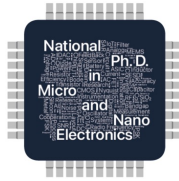UNIVERSITÀ DI PAVIA
Department of Electrical, Computer and Biomedical Engineering

National Ph.D. in Micro and Nano Electronics

National PhD School in Micro and Nano Electronics

Industrial Topics in Microelectronics and Photonics - Seminars

Introduction to Formal Verification of Digital Design and Jasper Apps: targeted solutions that address specific design and verification challenges

Abstract: The presentation is about Formal Verification methodology, probably the fastest growing digital design verification methodology. Formal is very different from simulation. Simulation is what is called zero-plus. You start with nothing, and you add some vectors. Then you add some more. It is hard to reach your verification target, even with a mixture of random and directed tests. On the other hand, formal is infinity-minus. You start with 100% by virtue of the technology, but there are false failures and failures to converge, so you add constraints. You can reach the point where the design is actually over-verified. A big challenge is that Formal algorithms are exponential. It may take two hours to verify 90 cycles, but four hours to verify 91, and to push up to 100 cycles, it may be measured in years.

The presentation will first introduce Formal Verification methodology and then shortly show how Cadence Jasper automated Apps can help to deploy Formal for particular verification tasks, where the formal properties are created automatically. Formal apps provide exhaustive verification with simple setup, so they can save many weeks of verification effort and increase design quality by finding more bugs at an earlier stage, compared with other verification methods.

Speaker: Massimo Roselli

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Massimo Roselli is a Digital Design & Verification Application Engineer Architect at Cadence Design System with 26 years' experience in Electronic Design Automation. Prior to Cadence, he worked as a Digital Designer and Verification Engineer for Galileo Avionica (now Leonardo). Massimo holds Electronic Engineering degree (MSEE) in Microelectronic from Università degli Studi di Roma "Tor Vergata".
Massimo has over 22 years of experience in Formal Verification. Massimo also has a deep knowledge of System on Chip and IP Verification with advanced testbench, complex RTL and Gate Level design debug, Low Power Design and Verification. He knows all common languages used for RTL Design and Verification including property specification languages.